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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,917	02/09/2004	Olivier Rayssac	4717-13100	1187

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

8/1

Office Action Summary	Application No.	Applicant(s)	
	10/775,917	RAYSSAC ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed December 23, 2005. Claims 1-20 are pending, in which claim 20 has been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Matsui et al (6,191,007).

Re claim 19 Matsui teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material, the wafer (118 in Fig 22) having first and second opposing faces, which comprises: providing at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) on the first face of the wafer; implanting atomic species through the second face and into the wafer to obtain a zone 120 of weakness at a predetermined depth therein (Fig 22, col 34, line 57 through col 35; col 28, lines 38-52; col 34, lines 25-55), the zone defining a first portion of the wafer extending from the zone to the first face and a remaining portion constituted by the remaining portion of the wafer; removing the remaining portion from the first portion along the zone of weakness to thin the wafer (Figs 2C,3C,210-22); wherein, not necessary to perform the last step of repeating the implanting and removing steps until the first portion has a reduced thickness that corresponds to a desired thickness for constituting a self-supported thin layer for the electronic component or circuit.

Claim Rejections - 35 USC § 103

2. Claims 1-4,7-11,16-18,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Hanson et al(5,920,764).

Matsui teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material, the wafer (118 in Fig 22) having first and second opposing faces, which comprises: providing at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34) on the first face of the wafer; implanting atomic species through the second face and into the wafer to obtain a zone 120 of weakness at a

predetermined depth therein (Fig 22, col 34, line 57 through col 35; col 28, lines 38-52; col 34, lines 25-55), the zone defining a first portion of the wafer extending from the zone to the first face and a remaining portion constituted by the remaining portion of the wafer; removing the remaining portion from the first portion along the zone of weakness to thin the wafer (Figs 2C,3C,210-22). Re claim 2, thinning the wafer by a mechanical polishing method is prior to the implanting of the atomic species (col 35, lines 21-28). Re claim 3, Matsui also teaches providing at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) on the first face of the wafer prior to the implanting of the atomic species. Re claim 4, wherein the remaining portion of the wafer is removed by applying a heat treatment (col 13, lines 60 through col 14). Re claim 7, wherein applying a stiffener (Fig 2C; 6,8,5) to the second face of the wafer 1 prior to removing the remaining portion by the application of a heat treatment (col 12, lines 40 through col 13; col 13, line 60 through col 14). Re claim 8, wherein the stiffener 6 is formed by deposition (col 12, lines 40-48). Re claim 9, wherein the stiffener 5 comprises a layer of silicon oxide (col 12, lines 35-48; Fig 2C). Re claim 10, wherein the stiffener 8,5,6 comprises a rigid plate (col 12, line 35 through col 13; col 25, lines 23-25). Re claim 11, wherein the rigid plate comprises a monocrystalline (col 13, lines 25-32) or polycrystalline silicon material (col 12, lines 40-48). Re claim 16, wherein the wafer comprises silicon (col 11, line 65 through col 12, line 8). Re claim 17, wherein the wafer comprises a silicon on insulator wafer (col 11, lines 60-65; col 35, lines 60-67; col 17, lines 29-50). Re claim 18, wherein the wafer comprises germanium, an alloy of silicon and germanium, silicon carbide (col 64, lines 49-56). Re further claim 20, Matsui also teaches removing the remaining portion as a self-supporting layer having a thickness of less than 35 micron from the first portion along the zone of weakness to thin the wafer (10 to several tens of microns at col 62, lines 1-8; 1-47; Fig 64D; 0.1 to 2 microns at col 15, lines 11-20).

Re claim 1, Matsui lacks mentioning the last step of claim 1 that, if necessary, repeating the implanting and removing steps until the first portion has a reduced thickness.

However, Hanson teaches (at Figs 4-5,3,1; col 4, lines 37-40; col 1, line 1 through col 2; col 4, line 6 through col 5) performing a Smart-Cut process by implanting hydrogen into the wafer to form a zone of weakness, and removing the portion to thinning the wafer, wherein, if

required, the process of implantation, heating, and fracture can be repeated until the desired thickness are removed so as to retain a wafer having reduced thickness (col 4, lines 37-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thinning a wafer made of a semiconductor material of Matsui by repeating the implanting and removing steps until the desired thickness are removed first portion has a reduced thickness, if required and if necessary, the process of implantation, heating, and fracture can be repeated until the desired thickness are removed, as taught by Hanson. This is because of the desirability to thinning and reduce a wafer having a desired thickness so that a thin wafer and small semiconductor devices can be fabricated.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Hanson et al (5,920,764), as applied to claims 1-4,7-11,16-18 above, and further of Henley (6,291,314).

The references including Matsui and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18 above.

Re claim 5, as described above, the references already teach removing the remaining portion of the wafer by heating, but lack blowing a jet of fluid adjacent the zone of weakness.

However, Henley teaches (at Fig 14; col 19, line 51 through col 21) removing the remaining portion by heating or blowing a jet of fluid adjacent the zone of weakness (col 20, 62 through col 21; col 20, lines 35-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to removing the remaining portion of the wafer of Matsui by heating or blowing a jet of fluid adjacent the zone of weakness, as taught by Henley, because these removing techniques are alternative and art recognized equivalent methods for removing a portion of the wafer in an effective and reliable manner.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Hanson et al (5,920,764), as applied to claims 1-4,7-11,16-18 above, and further of Kang et al (6,287,941).

The references including Matsui and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18 above.

Re claim 6, as described above, the references already teach removing the remaining portion of the wafer, but lack mentioning to remove the portion by scrubbing.

However, Kang et al teach (at col 9, lines 35-38; col 9,lines 14-67) to remove a portion o the wafer by scrubbing using a chemical mechanical polishing apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove a portion of the wafer of the references including Matsui by scrubbing with the use of a chemical mechanical polishing apparatus as taught by Kang, because scrubbing with the use of CMP polishing apparatus is an effective technique for removing a portion of the wafer in an effective manner so that leave a smooth surface.

5. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Hanson et al (5,920,764), as applied to claims 1-4,7-11,16-18 above, and further of Aspar et al (6,020,252) and Sayyah (2002/0055237).

The references including Matsui and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18 above.

As described above to claim 10, the references already teach applying a stiffener comprising a rigid plate 8,5,6 (Matsui, col 12, line 35 through col 13; col 25, lines 23-25), but lack to use a stiffener comprising a flexible film (claim 12) or an adhesive film (claim 13), a wax layer (re claim 14).

However, Aspar teaches (at col 6, lines 6-39; Figs 3-4) applying a stiffener 8 comprising a rigid or flexible support (re claim 12), wherein the stiffener comprises an adhesive film (claim 13, col 6, lines 12-18). Sayyah also teaches (at Figs 1c-1g; col 1, paragraphs 6,34-36) using a release stiffener layer comprising an adhesive or a wax layer (paragraph 0006).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove a portion of the wafer of the references including Matsui by applying a stiffener on the substrate, wherein applying a stiffener 8 comprising a rigid or flexible

support, wherein the stiffener comprises an adhesive film (col 6, lines 12-18), as taught by Aspar, wherein using an adhesive or a wax layer is further taught by Sayyah. This is because these stiffeners of rigid or flexible and adhesive or wax layers are alternative and art recognized equivalent materials that can be effectively used as a support and release layer during the step of removing a portion of the wafer.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Hanson (5,920,764), as applied to claims 1-4,7-11,16-18, and Aspar et al (6,020,252) and Sayyah (2002/0055237), to claims 12-14, and further of Nuyen (5,827751).

The references including Matsui and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18 above.

Re claim 15, the relied references already teach applying a stiffener, but lacks mentioning to remove the stiffener thereafter.

However, Nuyen teaches (at Fig 1-9) applying a stiffener 8,6 to the substrate prior to removal of the remaining portion, and removing the stiffener after having obtained the self-supported thin layer (Fig 9; col 4, lines 58-67; col 3, lines 54 through col 4).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove a portion of the wafer of the references including Matsui by applying a stiffener on the substrate prior to removal the portion, and thereafter removing the stiffener after having obtained the self-supported thin layer, as taught by Nuyen. This is because of the desirability to release and transfer the thin layer to a permanent substrate.

Response to Amendment

7. Applicant's remarks filed December 23, 2005 have been fully considered but they are not persuasive, and in view of the new ground(s) of rejection.

Applicant apparently remarked that Matsui forms extremely thin patterned layers having a thickness only about 0.1 to 2 microns, while the present invention is directed to have very thin self-supporting layers, i.e., less than 30 μm or about 35μm.

In response, this is noted and found unconvincing. First, note that nowhere in the claims requires the thin layers having a less than 30 μm or about 35μm in order to be a self-supporting layers. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Second, Matsui also teaches removing the remaining portion as a self-supporting layer having a thickness of less than 35 micron from the first portion along the zone of weakness to thin the wafer, wherein a thin layer has a thickness of about 10 microns to several tens of microns is disclosed at column 62, lines 1-8; 1-47; Fig 64D; with 0.1 to 2 microns at col 15, lines 11-20 ("several" is defined as being more than two or three but not many). This thin layer together with circuit layers on its first face is having a thickness for constituting a self-supported thin layer for the electronic component circuit formed thereon.

Applicant alleged that a "...support substrate is mentioned in the text and in the figures of Matsui...that the in layer is too thin to be considered as a self-supporting layer..."

In response, this is noted and found unconvincing. As mentioned above, Matsui also teaches forming a thin layer has a thickness of about 10 microns to several tens of microns ("several" is defined as being more than two or three but not many). Moreover, contradictory to applicant's remarks, Claim 15 also recites "applying a stiffener to a first face of the wafer...", which stiffener acts the same as a supporting substrate in Matsui.

Although forming an extremely thin layer having a thickness of about 0.1 to 2 microns is preferred by Matsui, forming a very thin layer having a thickness of about 10 microns to several tens of microns is also taught.

Especially, Matsui also teaches and recognizes (at Figure 22, col 34, line 56 through column 35; col 35, lines 12-28) that by implanting atomic species through a back side and into the wafer substrate 118, the ion implanted layer is formed in region extremely near the back side face when using the available implant apparatus (unless a special apparatus is used). In the combination of the references of Matsui and Hanson, by repeating the implanting and removing steps as obviously taught by Hanson for about 1 times, the thin self-supporting layer for the electronic component or circuit is already formed. By further repeating the implanting and removing steps, a thinner self-supporting layer for the electronic component or circuit is then

formed. Accordingly, an extremely thin layer having a thickness of about 0.1 to 2 microns of Matsui can be formed by repeating the implanting and removing steps for many times while a very thin self-supporting layer having a thickness of about 10 microns to several tens of microns can be obtained by repeating the implanting and removing steps for fewer times.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-17

Michael Trinh
Primary Examiner